Radiation Hardened, High Performance Industry Standard Single-Ended Current Mode PWM Controller

ISL78840ASEH, ISL78841ASEH, ISL78843ASEH, ISL78845ASEH

The ISL7884xASEH is a high performance, radiation hardened drop-in replacement for the popular 28C4x and 18C4x PWM controllers suitable for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Its fast signal propagation and output switching characteristics make this an ideal product for existing and new designs.

Features include up to 13.2V operation, low operating current, 90µA typical start-up current, adjustable operating frequency to 1MHz, and high peak current drive capability with 50ns rise and fall times.

PART NUMBER	RISING UVLO	MAX. DUTY CYCLE
ISL78840ASEH	7.0	100%
ISL78841ASEH	7.0	50%
ISL78843ASEH	8.4V	100%
ISL78845ASEH	8.4V	50%

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the ordering information must be used when ordering.

Detailed Electrical Specifications for the ISL788xASEH are contained in SMD 5962-07249. A “hot-link” is provided on our website for downloading.

Applications

- Current Mode Switching Power Supplies
- Isolated Buck and Flyback Regulators
- Boost Regulators
- Direction and Speed Control in Motors
- Control of High Current FET Drivers

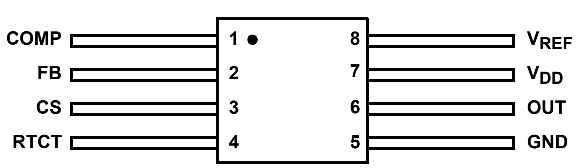
Features

- Electrically Screened to DLA SMD # 5962-07249
- QML Qualified Per MIL-PRF-38535 Requirements
- 1A MOSFET Gate Driver
- 90µA Typical Start-up Current, 125µA Max
- 35ns Propagation Delay Current Sense to Output
- Fast Transient Response with Peak Current Mode Control
- 9V to 13.2V Operation
- Adjustable Switching Frequency to 1MHz
- 50ns Rise and Fall Times with 1nF Output Load
- Trimmed Timing Capacitor Discharge Current for Accurate Deadtime/Maximum Duty Cycle Control
- 1.5MHz Bandwidth Error Amplifier
- Tight Tolerance Voltage Reference Over Line, Load and Temperature
- ±3% Current Limit Threshold
- Pb-Free Available (RoHS Compliant)
- Radiation Environment:
  - High Dose Rate (50 - 300rad(Si)/s). . . . . 100 krad(Si)
  - Low Dose Rate (0.01rad(Si)/s). . . . . . . 100 krad(Si) (Note)

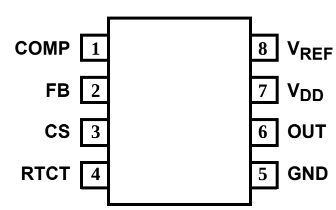
NOTE: Product capability established by initial characterization. The “EH” version is acceptance tested on a wafer by wafer basis to 50 krad(Si) at low dose rate.

Pin Configurations

ISL78840ASEH, ISL78841ASEH,
ISL78843ASEH, ISL78845ASEH
(8 LD FLATPACK)
TOP VIEW



ISL78840ASEH, ISL78841ASEH,
ISL78843ASEH, ISL78845ASEH
(8 LD SBDIP)
TOP VIEW



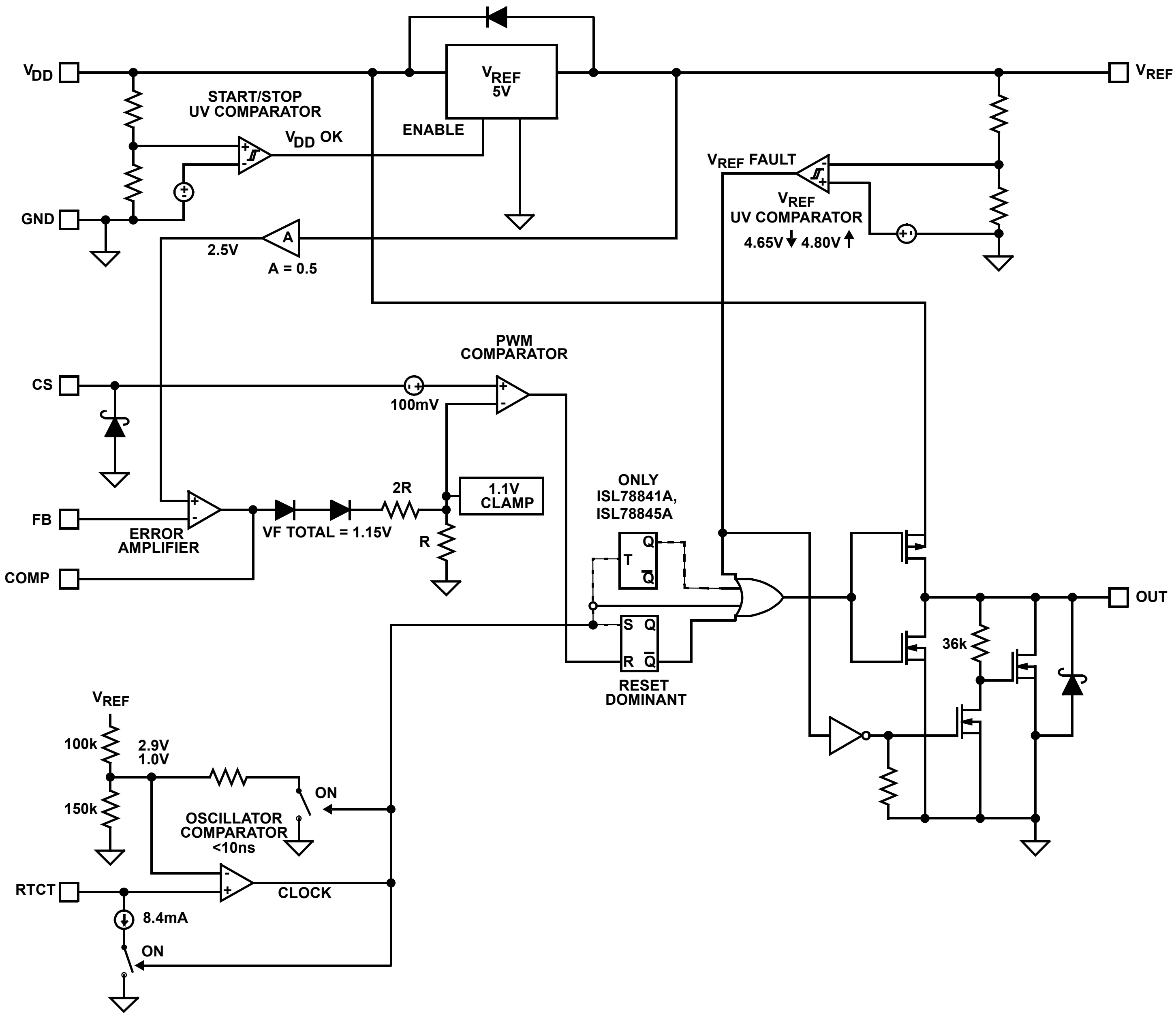
Ordering Information

ORDERING NUMBER	PART NUMBER (Notes 1, 2)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962R0724905VPC	ISL78840ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724906VPC	ISL78841ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724907VPC	ISL78843ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724908VPC	ISL78845ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724905VXC	ISL78840ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724906VXC	ISL78841ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724907VXC	ISL78843ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724908VXC	ISL78845ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724905V9A	ISL78840ASEHVX	-55 to +125	Die	
5962R0724906V9A	ISL78841ASEHVX	-55 to +125	Die	
5962R0724907V9A	ISL78843ASEHVX	-55 to +125	Die	
5962R0724908V9A	ISL78845ASEHVX	-55 to +125	Die	

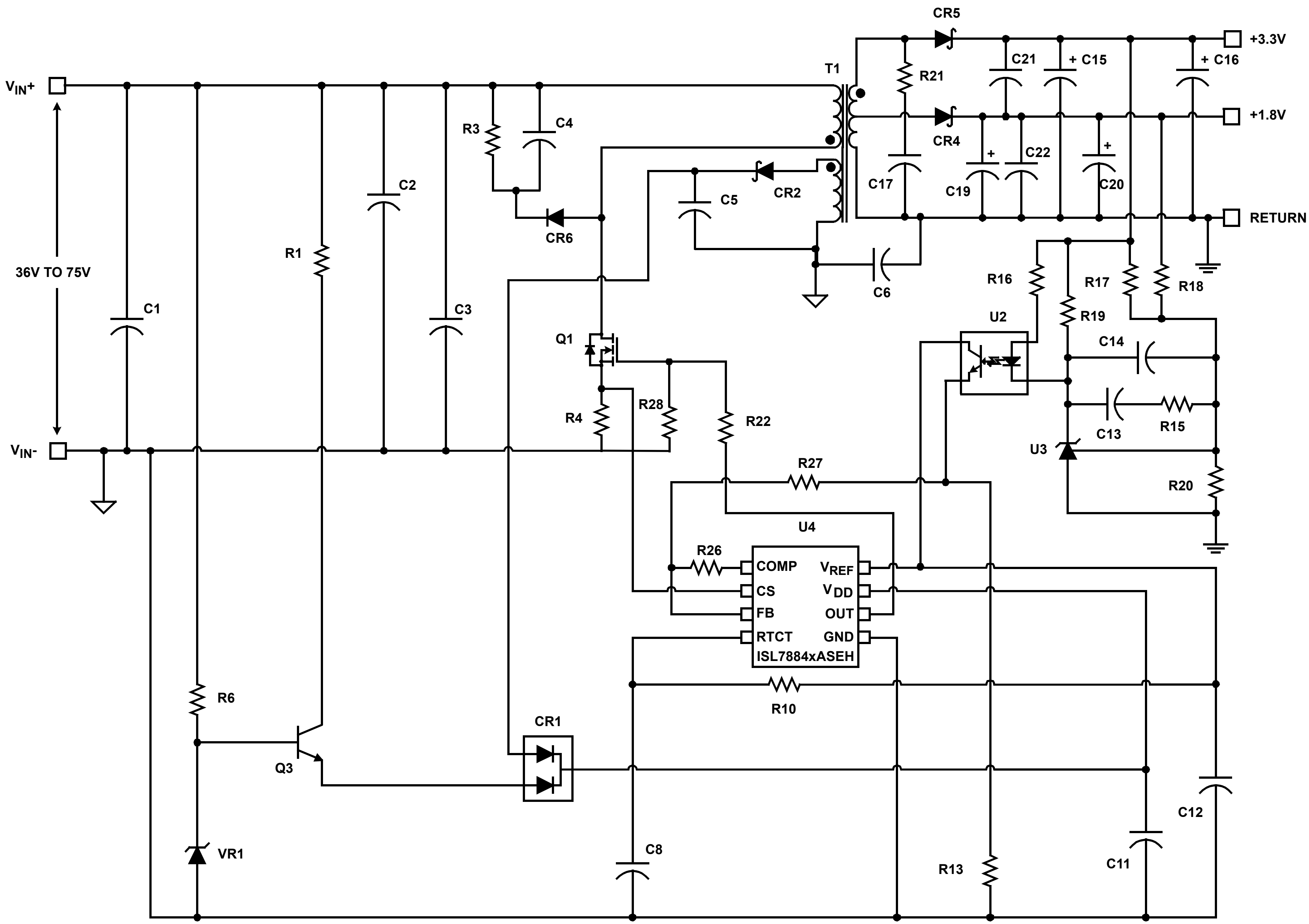
NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL78840ASEH, ISL78841ASEH, ISL78843ASEH, ISL78845ASEH. For more information on MSL please see techbrief TB363.

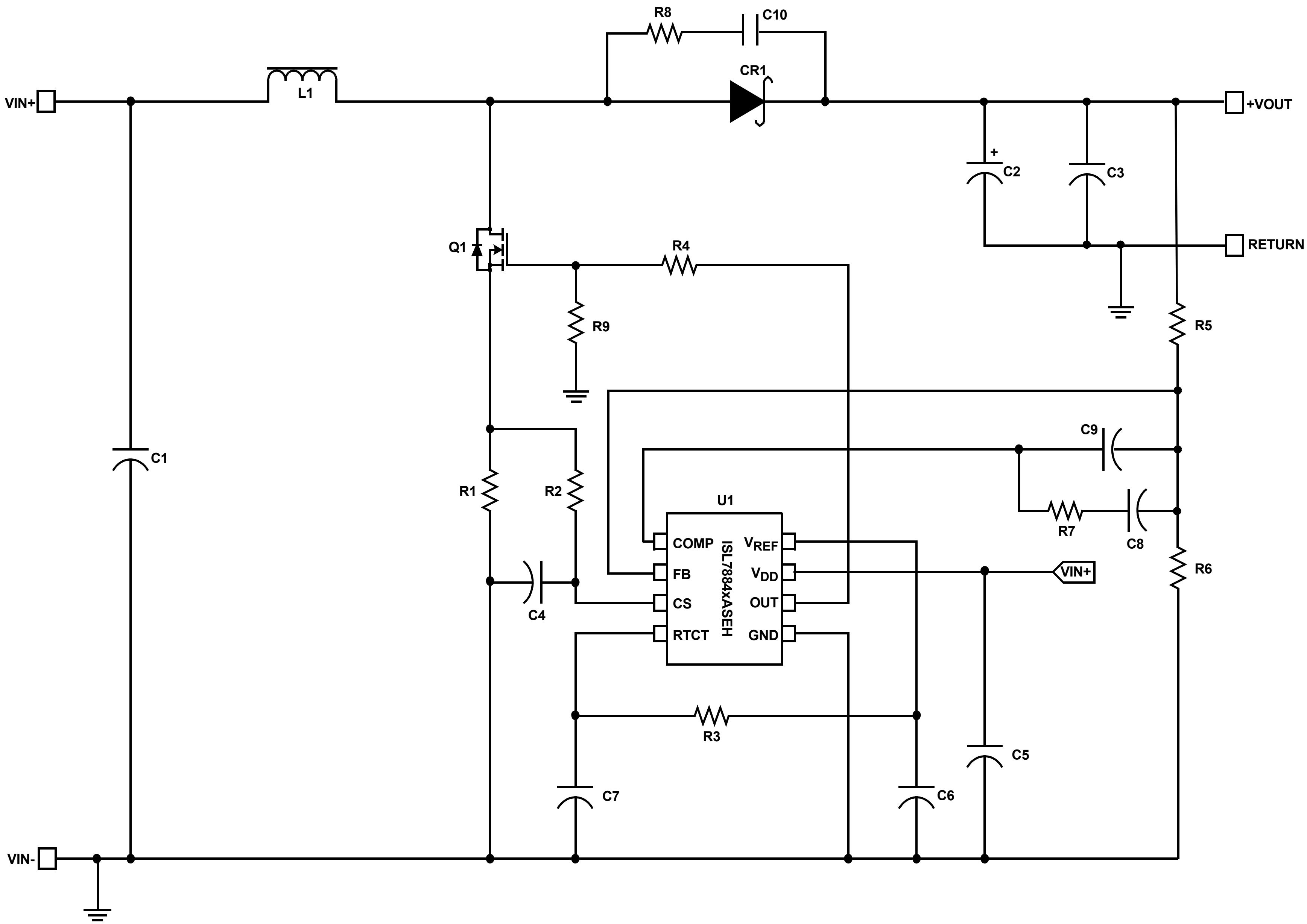
Functional Block Diagram



Typical Application - 48V Input Dual Output Flyback



Typical Application - Boost Converter



Absolute Maximum Ratings

Supply Voltage V_{DD} Without Beam . . . . .GND -0.3V to +30.0V
Supply Voltage V_{DD} Under Beam . . . . .GND -0.3V to +14.7V
OUT. . . . . GND -0.3V to V_{DD} + 0.3V
Signal Pins . . . . .GND -0.3V to 6.0V
Peak GATE Current 1A
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Recommended Operating Conditions

Temperature Range . . . .-55°C to +125°C
Supply Voltage (Typical Note 5) . . . . 9V to 13.2V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Flatpack Package (Notes 3, 4)	140	15
8 Ld SBDIP Package (Notes 3, 4)	98	15

Maximum Junction Temperature (Plastic Package) . . . .+150°C
Storage Temperature Range. . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Radiation Information

Maximum Total Dose
Dose Rate = 50 - 100radSi/s . . . . 100 krads (Si)
Dose Rate = 0.01rad(Si)/s (Note 6). . . . . 100 krad (Si)
SEB (No Burnout) (Note 6). . . . . 80Mev/mg/cm^2
SEL (No latchup) (Note 6) . . . . 80Mev/mg/cm^2
SET (Regulated V_{OUT} within ±3%) (Note 9) . . . . 40Mev/mg/cm^2

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.
5. All voltages are with respect to GND.
6. Product capability established by initial characterization. The “EH” version is acceptance tested on a wafer by wafer basis to 50 krad(Si) at low dose rate.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic on page 3 and page 4. V_{DD} = 13.2V, R_T = 10kΩ, C_T = 3.3nF, T_A = -55 to +125°C. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -55 to +125°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold	ISL78840A, ISL78841A	**6.5**	7.0	**7.5**	V
	ISL78843A, ISL78845A	**8.0**	8.4	**9.0**	V
STOP Threshold	ISL78840A, ISL78841A	**6.1**	6.6	**6.9**	V
	ISL78843A, ISL78845A	**7.3**	7.6	**8.0**	V
Hysteresis	ISL78840A, ISL78841A	-	0.4	-	V
	ISL78843A, ISL78845A	-	0.8	-	V
Start-up Current, I_{DD}	V_{DD} < START Threshold	-	90	**125**	µA
	V_{DD} < START Threshold, 100krad	-	300	**500**	µA
Operating Current, I_{DD}	(Note 7)	-	2.9	**4.0**	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.75	**5.5**	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 9V to 13.2V), load of 1mA and 10mA, temperature	**4.925**	5.000	**5.050**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 8)	-	5	-	mV
Current Limit, Sourcing		**-20**	-	-	mA
Current Limit, Sinking		**5**	-	-	mA
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	**-1.0**	-	**1.0**	µA
Input Signal, Maximum		**0.97**	1.00	**1.03**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic on page 3 and page 4. V_{DD} = 13.2V, R_T = 10kΩ, C_T = 3.3nF, T_A = -55 to +125°C. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -55 to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	$0 < V_{CS} < 910mV$, V_{FB} = 0V	**2.75**	2.82	**3.15**	V/V
CS to OUT Delay		-	35	**55**	ns
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 8)	-	90	-	dB
Unity Gain Bandwidth	(Note 8)	-	1.5	-	MHz
Reference Voltage, V_{REF}	$V_{FB} = V_{COMP}$	**2.475**	2.500	**2.530**	V
FB Input Bias Current, FBI_{IB}	V_{FB} = 0V	**-1.0**	-0.2	**1.0**	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	**1.0**	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	**-0.4**	-	-	mA
COMP VOH	V_{FB} = 2.3V	**4.80**	-	**V_{REF}**	V
COMP VOL	V_{FB} = 2.7V	**0.4**	-	**1.0**	V
PSRR	Frequency = 120Hz, V_{DD} = 9V to 13.2V (Note 8)	-	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_A = +25°C	**48**	51	**53**	kHz
Frequency Variation with V_{DD}	T_A= +25°C, $(f_{13.2V} - f_{9V})/f_{12V}$	-	0.2	**1.0**	%
Temperature Stability	(Note 8)	-	5	-	%
Amplitude, Peak-to-Peak	Static Test	-	1.75	-	V
RTCT Discharge Voltage (Valley Voltage)	Static Test	-	1.0	-	V
Discharge Current	RTCT = 2.0V	**6.5**	7.8	**8.5**	mA
OUTPUT					
Gate VOH	V_{DD} to OUT, I_{OUT} = -100mA	-	1.0	**2.0**	V
Gate VOL	OUT to GND, I_{OUT} = 100mA	-	1.0	**2.0**	V
Peak Output Current	C_{OUT} = 1nF (Note 8)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF	-	35	**60**	ns
Fall Time	C_{OUT} = 1nF	-	20	**40**	ns
OUTPUT OFF state leakage	V_{DD} = 5V	-	-	**50**	µA
PWM					
Maximum Duty Cycle (ISL78840A, ISL78843A)	COMP = V_{REF}	**94.0**	96.0	-	%
Maximum Duty Cycle (ISL78841A, ISL78845A)	COMP = V_{REF}	**47.0**	48.0	-	%
Minimum Duty Cycle	COMP = GND	-	-	**0**	%

NOTES:

7. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
8. Limits established by characterization and are not production tested.
9. SEE tests performed with VREF bypass capacitor of 0.22µF and F_{SW} = 200kHz. SEB/L tests done on a standalone open loop configuration. SET tests done in a closed loop configuration. For SEL no hard latch requiring manual intervention were observed. For more information see: ISL7884xASRH SEE Test Report.
10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

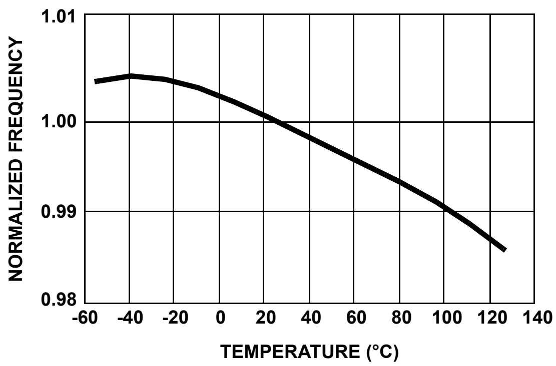


FIGURE 1. FREQUENCY vs TEMPERATURE

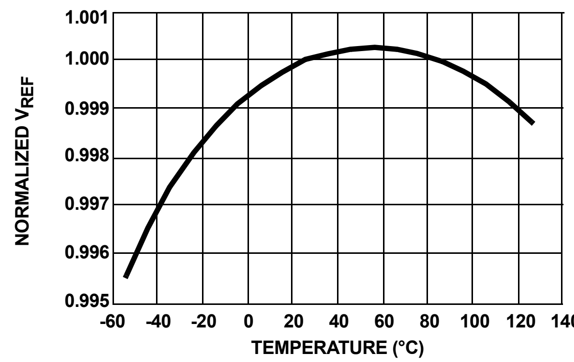


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

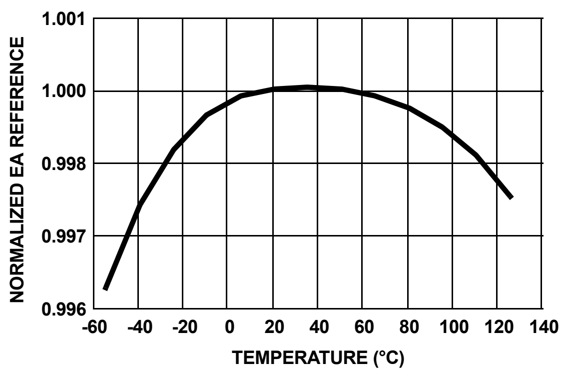


FIGURE 3. EA REFERENCE vs TEMPERATURE

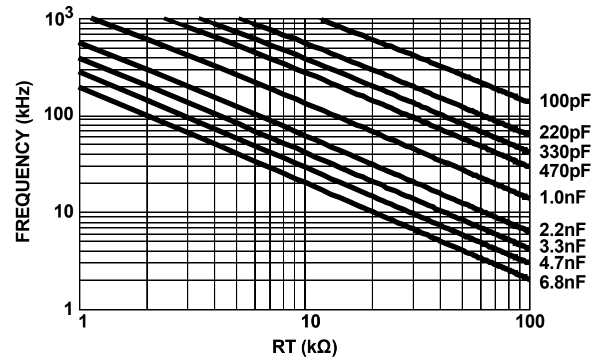


FIGURE 4. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

Pin Descriptions

RTCT - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between V_{REF} and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, t_C, the discharge time, t_D, the switching frequency, f, and the maximum duty cycle, D_{MAX}, can be approximated from Equations 1 through 4:

$$t_C \approx 0.533 \cdot RT \cdot CT \quad \text{(EQ. 1)}$$

$$t_D \approx -RT \cdot CT \cdot \ln\left(\frac{0.008 \cdot RT - 3.83}{0.008 \cdot RT - 1.71}\right) \quad \text{(EQ. 2)}$$

$$f = 1/(t_C + t_D) \quad \text{(EQ. 3)}$$

$$D = t_C \cdot f \quad \text{(EQ. 4)}$$

The formulae have increased error at higher frequencies due to propagation delays. Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given switching frequency for the ISL78841ASEH, ISL78845ASEH. The value for the ISL78840ASEH, ISL78843ASEH will be twice that shown in Figure 4.

COMP - COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.

FB - The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.

CS - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.

GND - GND is the power and small signal reference ground for all functions.

OUT - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{DD} is below the UVLO threshold.

V_{DD} - V_{DD} is the power connection for the device. The total supply current will depend on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated from Equation 5:

$$I_{OUT} = Qg \times f \quad \text{(EQ. 5)}$$

To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the V_{DD} and GND pins as possible.

V_{REF} - The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. The recommended bypass to GND cap is in the range 0.1µF to 0.22µF. A typical value of 0.15µF can be used.

Functional Description

Features

The ISL7884xASEH current mode PWM makes an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

Oscillator

The ISL7884xASEH has a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from V_{REF} and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency).

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated below, clamps the voltage on COMP.

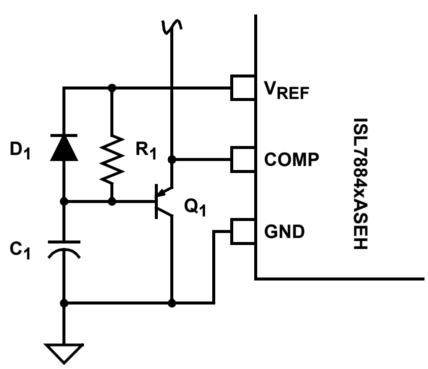


FIGURE 5. SOFT-START

The COMP pin is clamped to the voltage on capacitor C_1 plus a base-emitter junction by transistor Q_1. C_1 is charged from V_{REF} through resistor R_1 and the base current of Q_1. At power-up C_1 is fully discharged, COMP is at ~0.7V, and the duty cycle is zero. As C_1 charges, the voltage on COMP increases, and the duty cycle increases in proportion to the voltage on C_1. When COMP reaches the steady state operating point, the control loop takes over and soft-start is complete. C_1 continues to charge up to V_{REF} and no longer affects COMP. During power-down, diode D_1 quickly discharges C_1 so that the soft-start circuit is properly initialized prior to the next power-on sequence.

Gate Drive

The ISL7884xASEH is capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance. TID environment of >50krads requires the use of a bleeder resistor of 10k from the OUT pin to GND.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability.

Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain, Fm, without slope compensation is calculated in Equation 6:

$$Fm = \frac{1}{Sntsw} \quad \text{(EQ. 6)}$$

where Sn is the slope of the sawtooth signal and tsw is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes Equation 7:

$$Fm = \frac{1}{(Sn + Se)tsw} = \frac{1}{m_cSntsw} \quad \text{(EQ. 7)}$$

where Se is slope of the external ramp and becomes Equation 8:

$$m_c = 1 + \frac{Se}{Sn} \quad \text{(EQ. 8)}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at the switching frequency. The double-pole will be critically damped if the Q-factor is set to 1, over-damped for Q < 1, and under-damped for Q > 1. An under-damped condition may result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1-D)-0.5)} \quad \text{(EQ. 9)}$$

where D is the percent of on-time during a switching cycle. Setting Q = 1 and solving for Se yields Equation 10:

$$_e = S_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 10)}$$

Since Sn and Se are the on-time slopes of the current ramp and the external ramp, respectively, they can be multiplied by t_{ON} to obtain the voltage change that occurs during t_{ON}.

$$V_e = V_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 11)}$$

where V_n is the change in the current feedback signal (ΔI) during the on-time and Ve is the voltage that must be added by the external ramp.

For a flyback converter, Vn can be solved in terms of input voltage, current transducer components, and primary inductance, yielding Equation 12:

$$V_e = \frac{D \cdot T_{SW} \cdot V_{IN} \cdot R_{CS}}{L_p}\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1-D} - 1\right) \quad V \qquad \text{(EQ. 12)}$$

where R_{CS} is the current sense resistor, T_{sw} is the switching period, L_p is the primary inductance, V_{IN} is the minimum input voltage, and D is the maximum duty cycle.

The current sense signal at the end of the ON time for CCM operation is Equation 13:

$$V_{CS} = \frac{N_S \cdot R_{CS}}{N_P}\left(I_O + \frac{(1-D) \cdot V_O \cdot T_{sw}}{2L_s}\right) \quad V \qquad \text{(EQ. 13)}$$

where V_{CS} is the voltage across the current sense resistor, L_s is the secondary winding inductance, and I_O is the output current at current limit. Equation 13 assumes the voltage drop across the output rectifier is negligible.

Since the peak current limit threshold is 1.00V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold as:

$$V_e + V_{CS} = 1V \qquad \text{(EQ. 14)}$$

shown in Equation 14.

Substituting Equations 12 and 13 into Equation 14 and solving for R_{CS} yields Equation 15:

$$R_{CS} = \frac{1}{\frac{D \cdot T_{sw} \cdot V_{IN}}{L_p} \cdot \left(\frac{\frac{1}{\pi} + 0.5}{1-D} - 1\right) + \frac{N_s}{N_p} \cdot \left(I_O + \frac{(1-D) \cdot V_O \cdot T_{sw}}{2L_s}\right)} \qquad \text{(EQ. 15)}$$

Adding slope compensation is accomplished in the ISL7884xASEH using an external buffer transistor and the RTCT signal. A typical application sums the buffered RTCT signal with the current sense feedback and applies the result to the CS pin as shown in Figure 6.

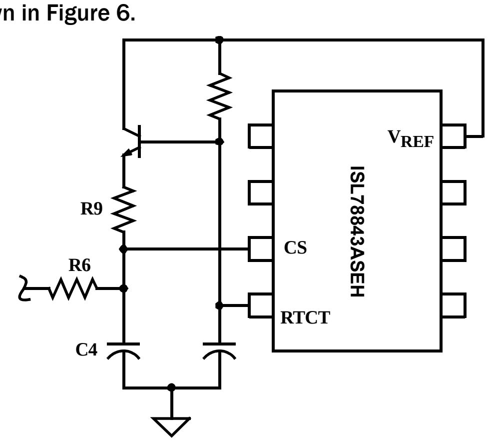


FIGURE 6. SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter (R_6 and C_4) placed on the CS pin, the value of R_9 required to add the appropriate external ramp can be found by superposition.

$$V_e = \frac{2.05D \cdot R_6}{R_6 + R_9} \quad V \qquad \text{(EQ. 16)}$$

The factor of 2.05 in Equation 16 arises from the peak amplitude of the sawtooth waveform on RTCT minus a base-emitter junction drop. That voltage multiplied by the maximum duty cycle is the voltage source for the slope compensation. Rearranging to solve for R_9 yields Equation 17:

$$R_9 = \frac{(2.05D - V_e) \cdot R_6}{V_e} \quad \Omega \qquad \text{(EQ. 17)}$$

The value of R_{CS} determined in Equation 15 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 13. The divider created by R_6 and R_9 makes this necessary.

$$R'_{CS} = \frac{R_6 + R_9}{R_9} \cdot R_{CS} \qquad \text{(EQ. 18)}$$

Example:

V_{IN} = 12V

V_O = 48V

L_s = 800µH

Ns/Np = 10

Lp = 8.0µH

I_O = 200mA

Switching Frequency, f_{SW} = 200kHz

Duty Cycle, D = 28.6%

R_6 = 499Ω

Solve for the current sense resistor, R_{CS}, using Equation 15.

R_{CS} = 295mΩ

Determine the amount of voltage, Ve, that must be added to the current feedback signal using Equation 12.

Ve = 92.4mV

Using Equation 17, solve for the summing resistor, R_9, from CT to CS.

R_9 = 2.67kΩ

Determine the new value of R_{CS} (R'_{CS}) using Equation 18.

R'_{CS} = 350mΩ

Additional slope compensation may be considered for design margin. The above discussion determines the minimum external ramp that is required. The buffer transistor used to create the external ramp from RTCT should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into RTCT and will reduce the oscillator frequency.

Fault Conditions

A Fault condition occurs if V_{REF} falls below 4.65V. When a Fault is detected, OUT is disabled. When V_{REF} exceeds 4.80V, the Fault condition clears, and OUT is enabled.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

References

[1] Ridley, R., “A New Continuous-Time Model for Current Mode Control”, IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

Package Characteristics

Weight of Packaged Device

8 Ld Mini DIP: 0.7004 Grams
8 Ld Flatpack: 0.3605 Grams

Die Characteristics

Die Dimensions

2030µm x 2030µm (80 mils x 80 mils)
Thickness: 482µm ± 25.4µm (19.0 mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ± 0.03µm to 1.2µm ± 0.12µm

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 2.7µm ±0.4µm

SUBSTRATE

Silicon

BACKSIDE FINISH

Silicon

PROCESS

0.6µM BiCMOS Junction Isolated

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased

ADDITIONAL INFORMATION

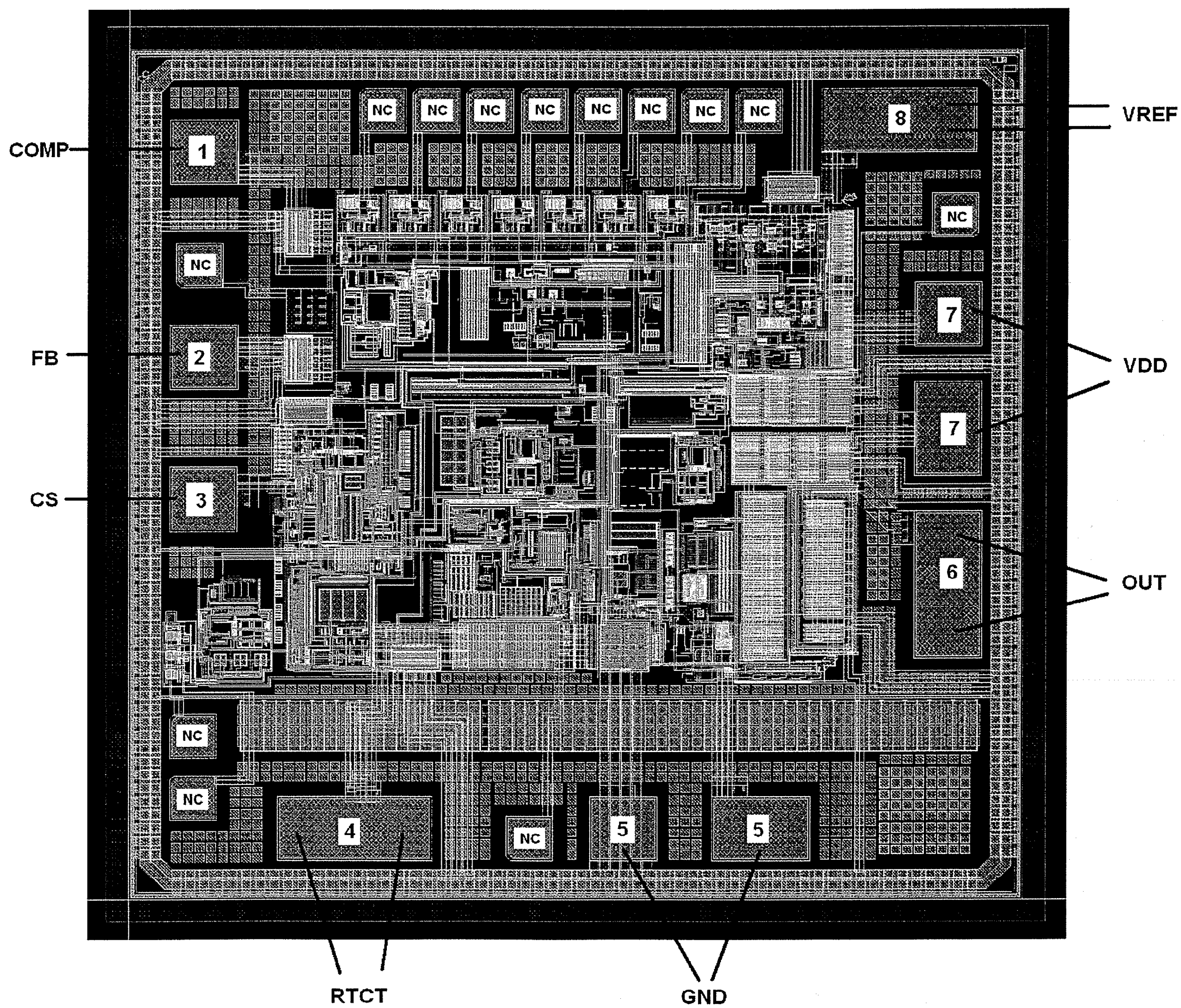
Worst Case Current Density

< 2 x 10^5 A/cm^2

Transistor Count

1278

Die Map



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
May 4, 2012	FN7952.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL78840ASEH, ISL78841ASEH, ISL78843ASEH, ISL78845ASEH

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

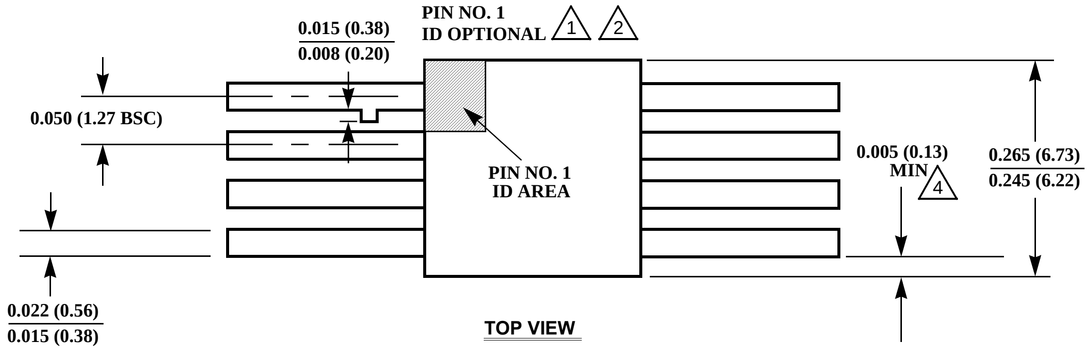
FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

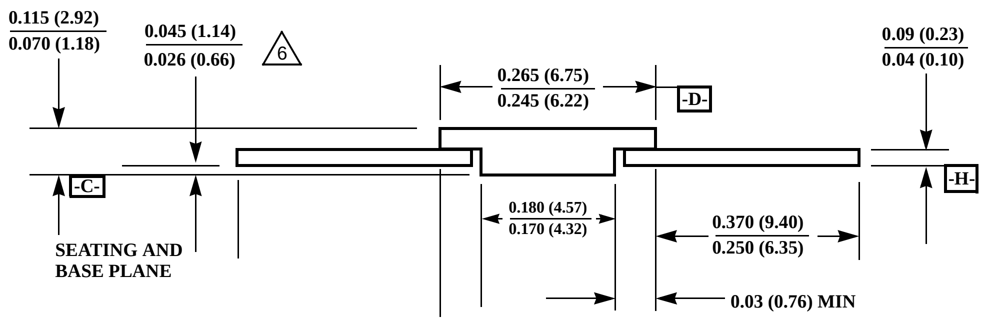
K8.A

8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

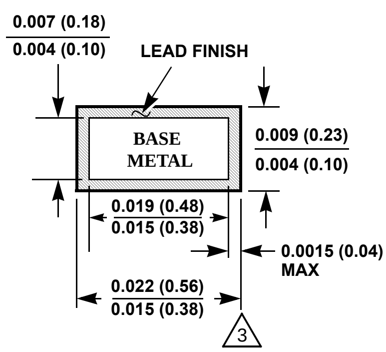
Rev 2, 12/10



TOP VIEW



SIDE VIEW

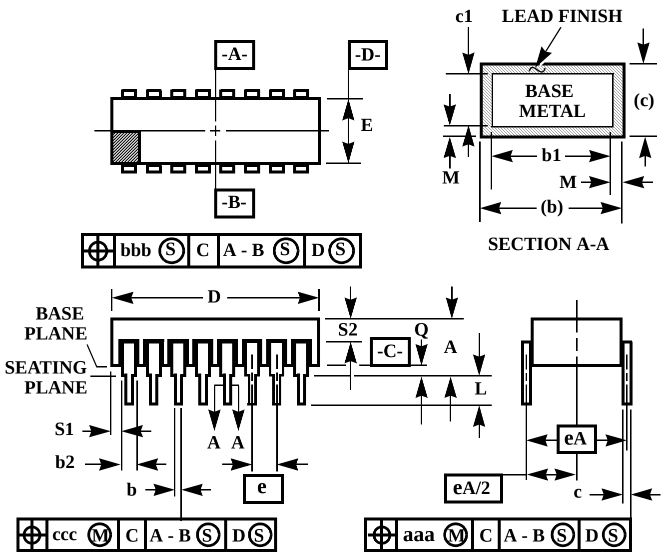


SECTION A-A

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.